REMARKS

In accordance with the foregoing, a substitute Abstract is presented, responsive to Item 1 of the Action, and claim 11 is amended responsive to the objection thereto in Item 2 of the Action.

Presented and, accordingly, approval and entry of the foregoing substitute Abstract and amended claim 11 are respectfully requested.

STATUS OF CLAIMS

Claims 1-10, 15-26, 42 and 44 are allowed.

Claims 11-14, 27-34 and 43 are objected to but indicated to be patentable if suitably rewritten to independent form.

Claims 11, 27 and 35 are rejected.

Claims 1-44 remain pending herein and reconsideration of the claims objected to and rejected are respectfully requested.

REQUEST FOR CORRECTION OF STATUS OF CLAIM 43

The status of claim 43, as specified in the Office Action Summary and in Item 12 of the Action and as listed above, is that it is objected to. Correction of the record appears appropriate.

Particularly, claim 43 depends from claim 22 - - and claim 22, both in the Office Action Summary and in Item 13, is indicated to be allowed. Accordingly, it is submitted that claim 43/22 likewise should be designated as allowed and such action is earnestly solicited.

ITEM 5: REJECTION OF CLAIM 11 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER TULPULE (U.S. PATENT 4,696,019) IN VIEW OF BRAUNS (U.S. PATENT 5,689,533)

The rejection is respectfully traversed.

Tulpule discloses a synchroniser 10 (FIG. 2). One such synchroniser 10 is associated individually with each of a plurality (N) of data processors 14, as shown in FIG. 1. Each synchroniser 10 has N inputs. One input corresponds to its own synchroniser 10 and the other inputs correspond to the remaining N-1 synchronisers. An incoming sync drive signal is received at each of the N inputs. The N sync drive signals are latched by input latches 26 and then supplied to a set of rising edge latches 32 and a set of falling edge latches 34. As the Examiner has noted, there are N latches in the set of rising edge latches 32 and N latches in the set of falling edge latches 34 (col. 5, lines 11-12 and col. 6, lines 6-7).

As indicated at col. 5, lines 12-13, each rising edge latch 32 is associated with one of the N incoming sync signals. In other words, there is a one-to-one correspondence between rising edge latches and incoming sync signals. All the rising edge latches are set temporarily into a responsive state by an enable signal on line 40, which establishes a time window during which each rising edge latch can detect a transition on its associated incoming sync signal. Accordingly, for each incoming sync signal that undergoes a transition during the time window, its associated rising edge latch will register the transition.

The circuitry which follows the rising edge latches 32 (the disable gating 48, voter #1 58 and MS arm latch 64) provides an arm signal if rising edges are detected on at least a selected number of incoming sync signals, for example on at least four sync signals. If, and only if, the arm signal is provided based on the outputs of the rising edge latches, the falling edge latches 34 are all enabled (col. 6, lines 17-21). The circuitry which follows the falling edge latches 34 (the disable gating 70, voter #2 86 and MS latch 84) produce a frame sync signal if falling edges are detected on at least the selected number of incoming sync signals.

The Examiner is therefore correct, in asserting that the synchroniser 10 in Tulpule has N rising-edge latches and N falling-edge latches as required by claim 11. However, the N rising-edge latches 32 in Tulpule correspond respectively to the inputs of the synchroniser, and the N falling edge latches 34 also correspond respectively to the inputs. By contrast, amended claim 11 requires the circuitry to be operable to perform a repeating series of N cycles, each cycle having a rising edge and a falling edge. The claim also requires a rising-edge latch and a falling-edge latch, per cycle, of the circuitry and that all the latches receive the same stream of data. Claim 11 also requires that each rising-edge latch is "triggered at said rising edge of a different one of the N cycles of the repeating series to take a rising-edge sample of the data". Similarly, claim 11 requires that each falling-edge latch is "triggered at said falling edge of a different one of the N cycles of said repeating series to take a falling-edge sample of data".

The recitations of amended claim 11 are graphically represented, and observable, in FIGS. 11(A) and 11(B), which show a repeating series of N cycles (N = 4 in this example). A first series of four cycles A0 to A3 is followed by a second series of cycles B0 to B3 and a third series of cycles C0 to C3. There is a rising edge latch (40 in FIG. 6) per cycle in each series, and a falling edge latch (42 in FIG. 6) per cycle in each series. Each latch 40 or 42 is connected to receive the same stream of data DIN. At the rising edge of cycle 0, in each series of cycles, only the rising edge latch 40_0 receives an active enable signal ENr0. The enable signals ENr1, ENr2 and ENr3 of the other rising edge latches 40_1, 40_2 and 40_3 are all inactive. Accordingly, at time J

in FIG. 11(B) the rising-edge latch 40_0 alone is triggered to take a sample of the data DIN. Similarly, at the falling edge in cycle 0 of each series of cycles (i.e. at time K in FIG. 11(B)), the falling-edge latch 40_0 alone is triggered to take a sample of the stream of serial data DIN. The next rising-edge sample is taken by the rising edge latch 40_1 at the rising edge of cycle 1, i.e. at time M in FIG. 11(B). The next falling-edge sample is taken by the falling-edge latch 42_1 at the falling edge in cycle 1, i.e. at time N.

The clock recovery circuitry, as defined by the amended claim 11, affords the advantage, although the rising and falling edge latches considered together take samples within half a clock cycle of one another, each latch is only updated once in every four clock cycles. For example, the latch 40_0 is next updated in cycle C0 of the next series of four cycles C0 to C3. This strategy allows about N-0.5 clock cycles (rather than 0.5 clock cycles as in previously-considered clock recovery circuitry) before the data samples must be transferred again to other latches or evaluated directly, which makes the further circuitry which processes the data samples much simpler to design (see specification page 28, lines 11-24). As noted above, in Tulpule each rising edge latch and each falling edge latch is associated with a different sync signal. Also, in Tulpule, the rising edge latches are all enabled at the same time (i.e., in the time window defined by the signal on the line 40). The falling edge latches are not enabled at all at this time. The falling edge latches are enabled together in the event that the number of incoming sync signals having rising edges during the time window is at least a selected number.

Neither the structural recitations of the amended claim 11, nor the advantageous functions afforded thereby, as discussed above, are discussed by Tulpule, whether taken singly or in combination with Brauns.

ITEM 8: REJECTION OF CLAIMS 27 AND 35 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER BUCKNER (U.S. PATENT 5,509,037) IN VIEW OF EILKEN (U.S. PATENT 6,445,252)

The rejections are respectfully traversed.

As stated by the Examiner in paragraph 9 of the Office Action, Buckner discloses a data recovery circuitry 34 for sampling a received serial data stream (e.g., D10), comprising a clock recovery circuit (FIG. 5) connected for receiving a plurality of candidate clock signals 01 to 05 having the same frequency but spaced apart, one from the next, in phase and operable to select, as a recovered clock signal, one of the candidate clock signals that matches the received serial data stream in phase (FIG. 4 and col. 4, lines 4-9). However, Buckner does not disclose an offset clock circuit operable to select, as an offset clock signal, a further one of said

candidate clock signals, different from said candidate clock signal selected as said recovered clock signal, nor does Buckner disclose a data sampling circuit operable to sample said received data stream using said offset clock signal.

Eilken discloses (FIG. 3) an offset unit OU arranged in a control unit CU of a digital phase lock loop DPLL. The offset unit OU comprises a memory unit SE and a synchronous counter SC. A register value RV and an increment value CV are stored in the memory unit SE (Eilken, col. 8, lines 61-63). It appears that the offset unit controls the generation of first and second recovered output clock signals es_{CLK1} and es_{CLK2}. The first recovered output clock signal es_{CLK1} is applied to a first buffer memory PS1 in an input unit IU to control the reading of an incoming data signal ds into the first buffer memory. The second recovered output clock signal es_{CLK2} is applied to a second buffer memory PS2 in an output unit EU in order to control the reading out of a data signal ds from the second buffer memory. Each of these first and second recovered output clock signals is said to "exhibit an offset with respect to the reference signal rs" (col. 9, lines 15-16) and col. 9, line 55). However, it appears that the offset is a frequency offset in Eilken whereas, in the present invention, the offset clock signal has the same frequency as the recovered clock signal but merely differs from the recovered clock signal in phase: see Eilken, col. 2, lines 49-51, col. 3, lines 5-8, col. 9, lines 10-13 and col. 9, lines 24-28. Original claim 27 clearly specifies that the plurality of candidate clock signals have the same frequency but are spaced apart one from the next in phase. Accordingly, because the offset clock signal is a different one of the candidate clock signals from the recovered clock signal, it follows that the offset clock signal must have the same frequency as the recovered clock signal. Thus, claim 27 is submitted to distinguish over Eilken.

The present invention is founded on the inventive recognition that the recovered clock signal may not be the optimum clock signal to use to sample the received data stream. Still further, the present invention provides a highly effective way of obtaining the offset clock signal without involving significant extra hardware, by utilizing a different one of the candidate clock signals as the offset clock signal. Claim 27 is therefore is submitted to distinguish patentably over Buckner, whether taken alone or in combination with Eliken.

It is respectfully submitted that such teachings are altogether absent from the disclosures of any of the references.

The Examiner has stated that it would be obvious to combine the teachings of Buckner and Eilken to arrive at the data recovery circuitry of claim 27. However, insofar as Eilken can be regarded as teaching the use of two different recovered output clock signals, it does so in the

context of managing the reading of data from, and the writing of data into, two different buffers. Eilken teaches nothing in relating to the shape of the data eye, and does not lead in any way to an appreciation that, depending on the shape of the data eye, it may be better to sample the received data stream using an offset clock signal which has the same frequency but differs in phase from the recovered clock signal produced by the clock recovery circuit (DPLL). Accordingly, the alleged motivation to combine the two references referred to by the Examiner in paragraph 10 of the Office Action does not exist.

PRIMA FACIE OBVIOUSNESS OF THE PRIOR ART COMBINATIONS HAS NOT BEEN DEMONSTRATED

The rejections in each of Items 5 and 8 of the Action rely on the contention really that "it would have been obvious..." to combine the teachings of the respective pairs of references, essentially on the grounds that "one of ordinary skill in the art..." would have been motivated to combine the respective teachings - - in the case of Item 5 and Tulpule and Brauns, both suggest use of clock synchronizing and, in the case of Buckner and Eilken in Item 8, both have sampling circuits operable to sample received data streams using offset clock signals or that both teach aligning data with one of the phases of the clock signals as to Buckner or suggest the beneficial use of the aligning data with two phases of a clock as in the case of Eilken. Merely citing examples of the teachings does not amount to defining motivation in the references to effect the combination of both. MPEP 2143-2143.03.

CONCLUSION

It is respectfully submitted that the pending claims 11, 25 and 35 have been shown to distinction patentably over the references of record. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS:

The attached Replacement sheet of FIG. 6 corrects/adds reference numerals to the edge latch; a copy of FIG. 6 annotated to indicate the corrected/added reference numerals is enclosed also.

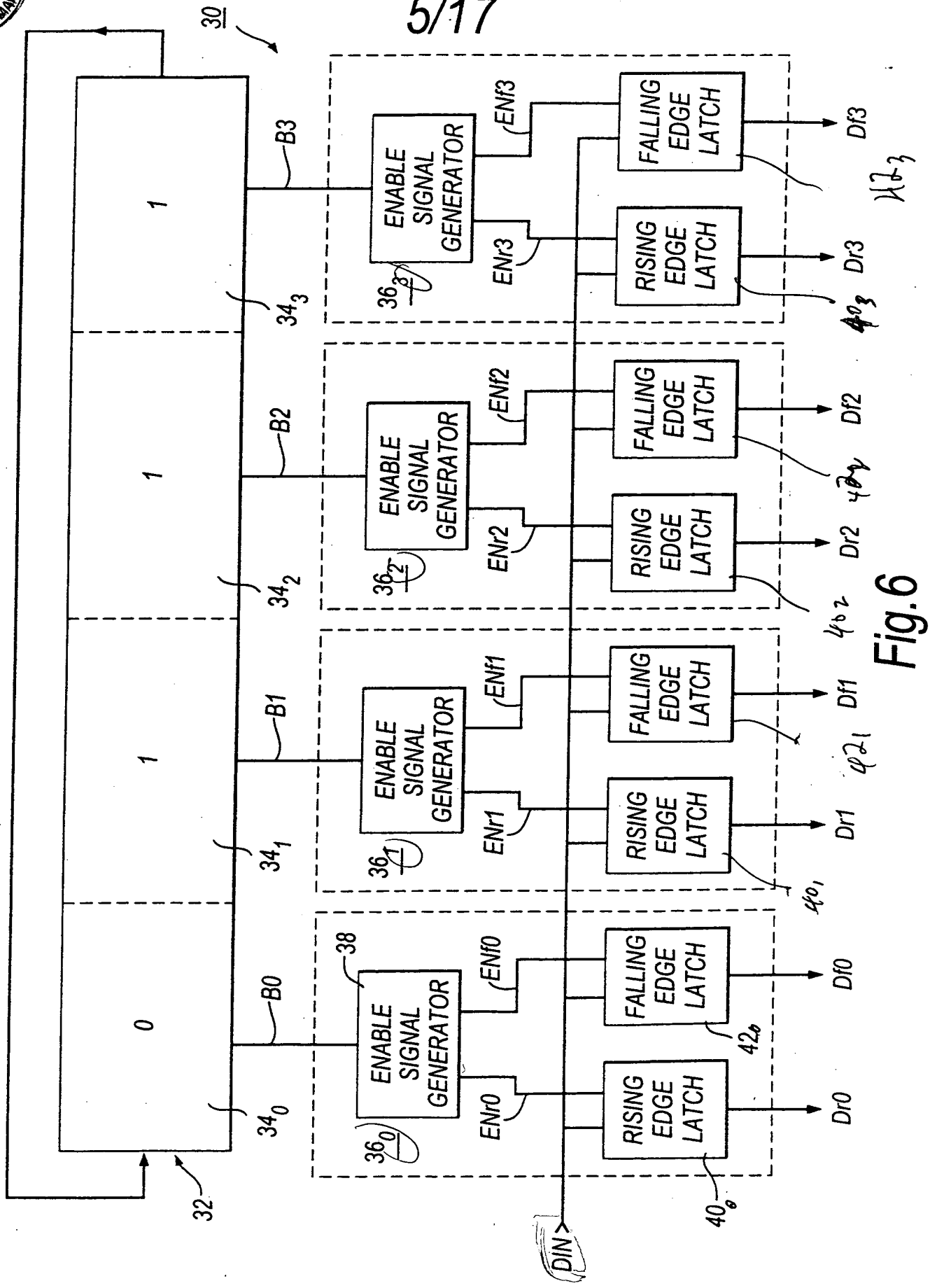

Fig.6